

Intel's Next-Generation Logic Process Proven With World-Record Memory Chip

What are we announcing?

- **A significant milestone achieved towards delivery of 90 nm (0.09 μm) process technology**
- **Produced fully-functional SRAM chips, the standard test vehicle for a new logic process**
 - **1 μm^2 cell size, first to reach this industry milestone**
 - **52 Mbit, highest capacity ever reported**
 - **330 million transistors, on road to 1 billion transistor CPU**
- **These SRAM chips demonstrate all the 90 nm process features required for microprocessors, including transistors and 7 Cu interconnect layers**
- ***Not a paper announcement ... this silicon is real and fully functional***

Why is this important?

- Shows that Intel is on track, delivering a new process technology every 2 years
- Each new generation allows higher clock rates and more transistors at lower cost, delivering more value to the end user
- World's smallest SRAM cell, at $1\ \mu\text{m}^2$, illustrates Intel's ability to build very large caches and very high density logic for maximum performance
- This development will enable products with higher performance that use less power

A new process every 2 years

Process Name	<u>P854</u>	<u>P856</u>	<u>P858</u>	<u>Px60</u>	<u>P1262</u>	<u>P1264</u>
1 st Production	1995	1997	1999	2001	2003	2005
Lithography	0.35μm	0.25μm	0.18μm	0.13μm	90nm	65nm
Gate Length	0.35μm	0.20μm	0.13μm	<70nm	<50nm	<35nm

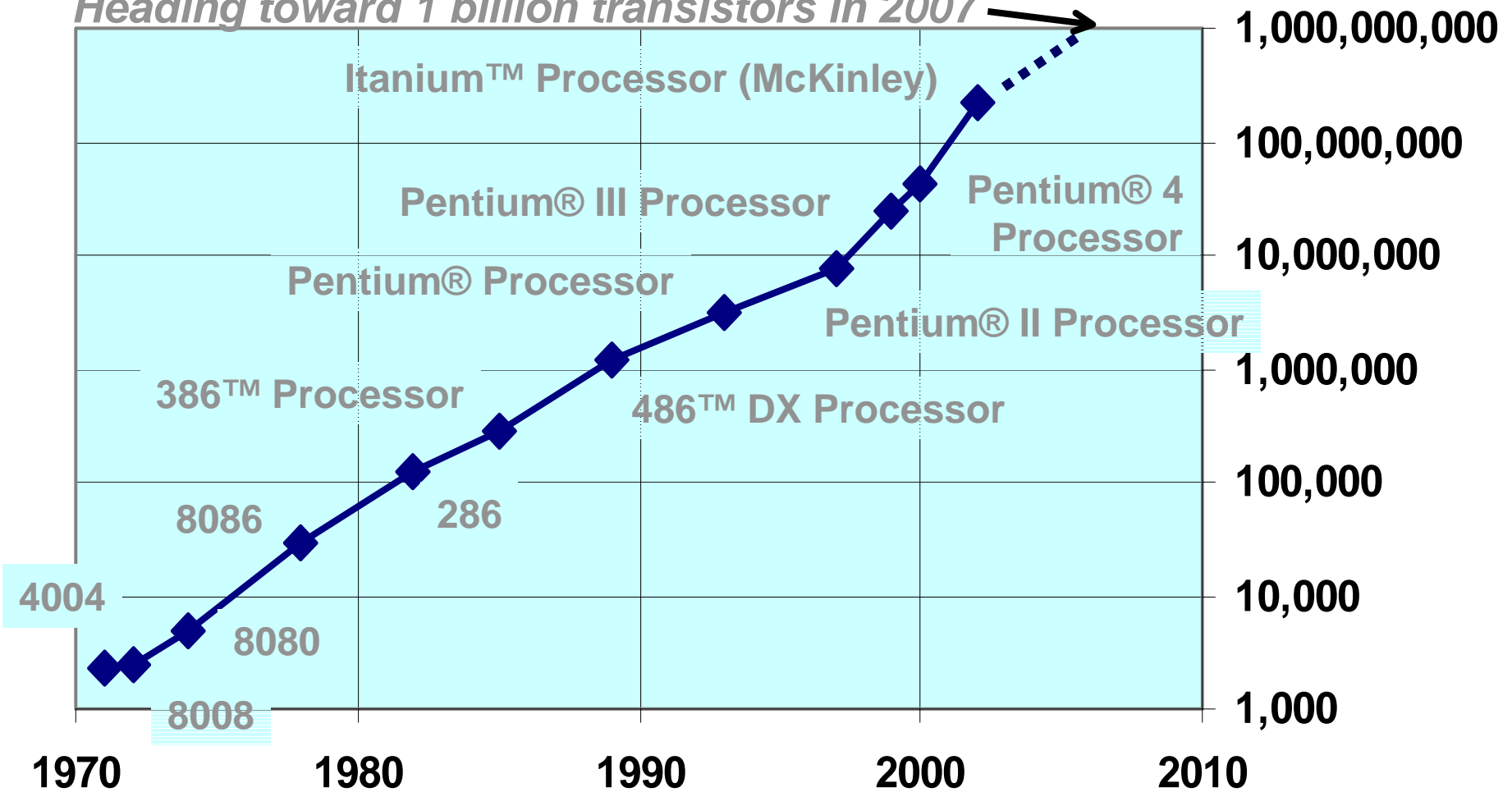
*The first product on 90 nm will be Prescott CPU,
as disclosed recently at the Intel Developer Forum*

Moore's Law

- **Doubling of number of transistors per integrated circuit every 18-24 months**
 - First observed in 1965
 - Intel expects to continue at least through end of this decade
- **This expectation has driven our research, development, and investments for the last 3 decades**
 - Has enabled the incredible price/performance progress of the electronics industry

Moore's Law Continues

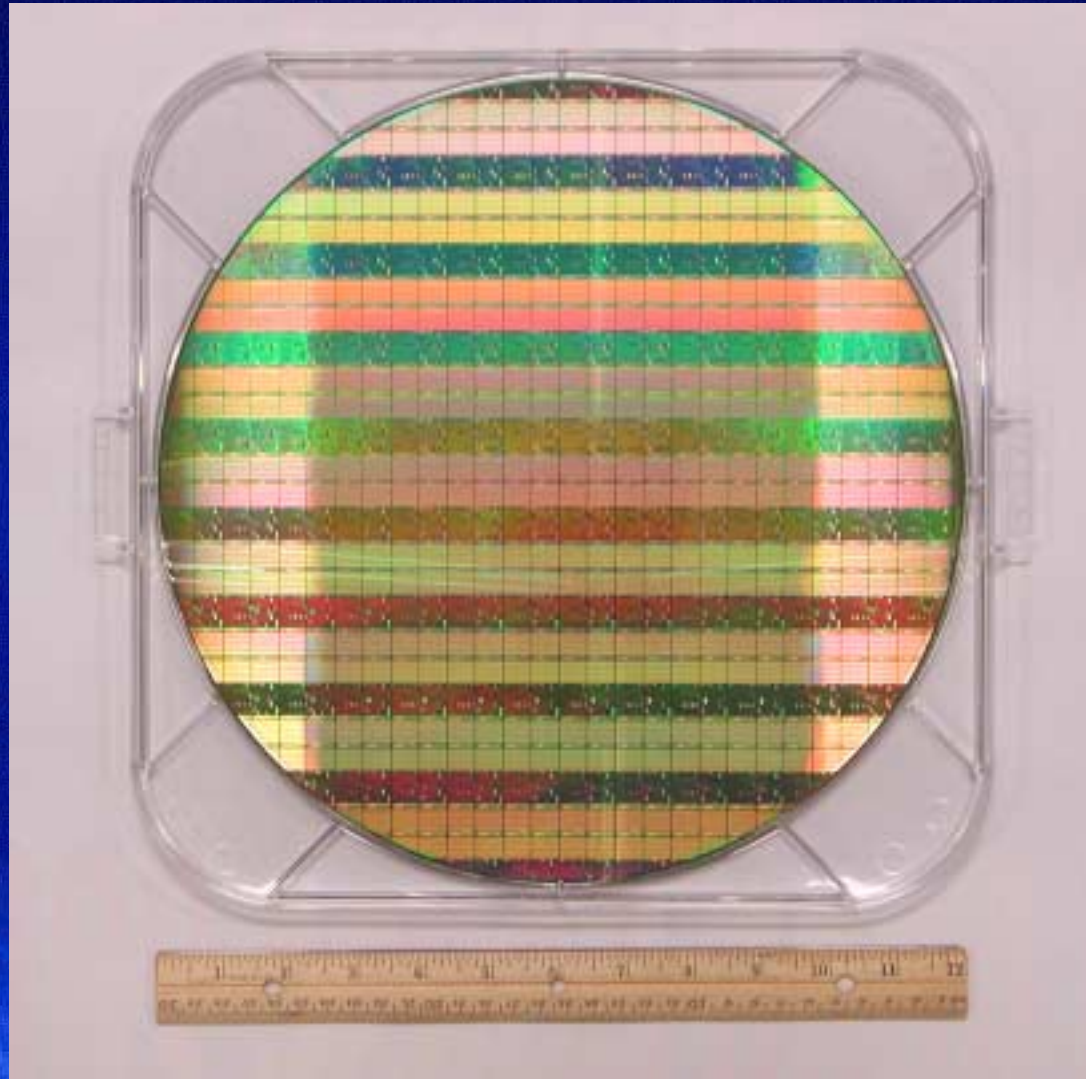
Heading toward 1 billion transistors in 2007



This chip contains 330 million transistors

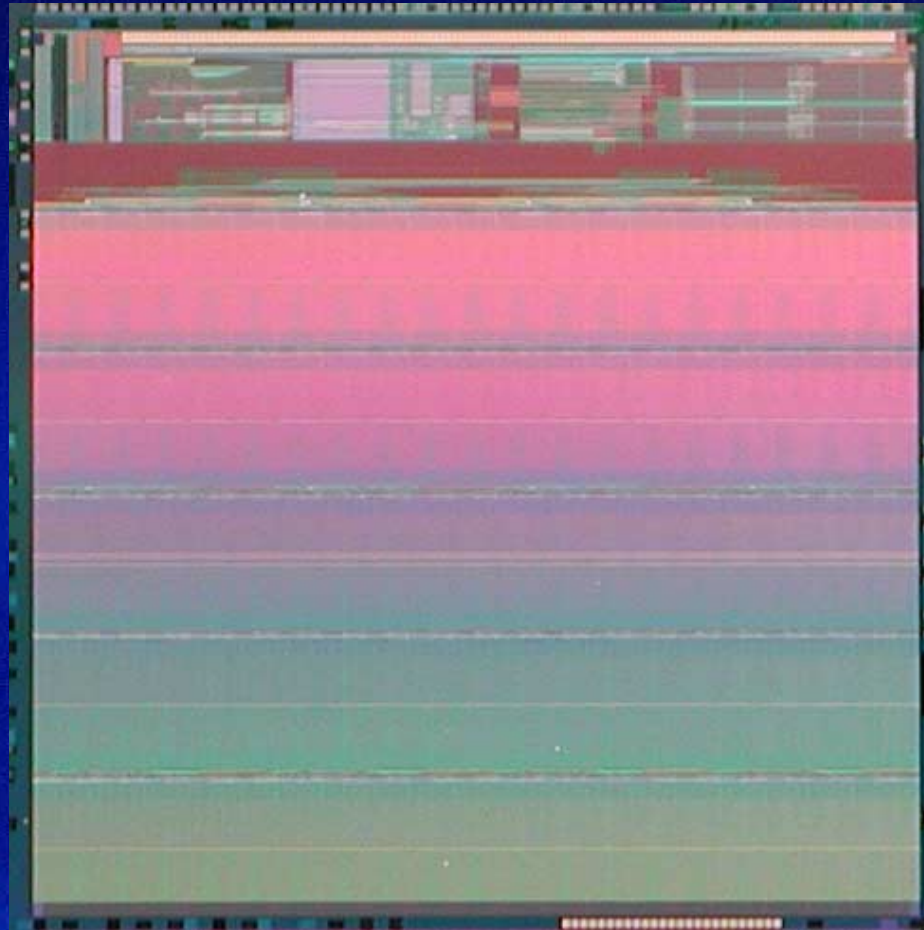
90 nm Chip Produced on 300 mm Wafer

120 billion transistors on one wafer!



Fully-Functional 52 Mbit SRAM

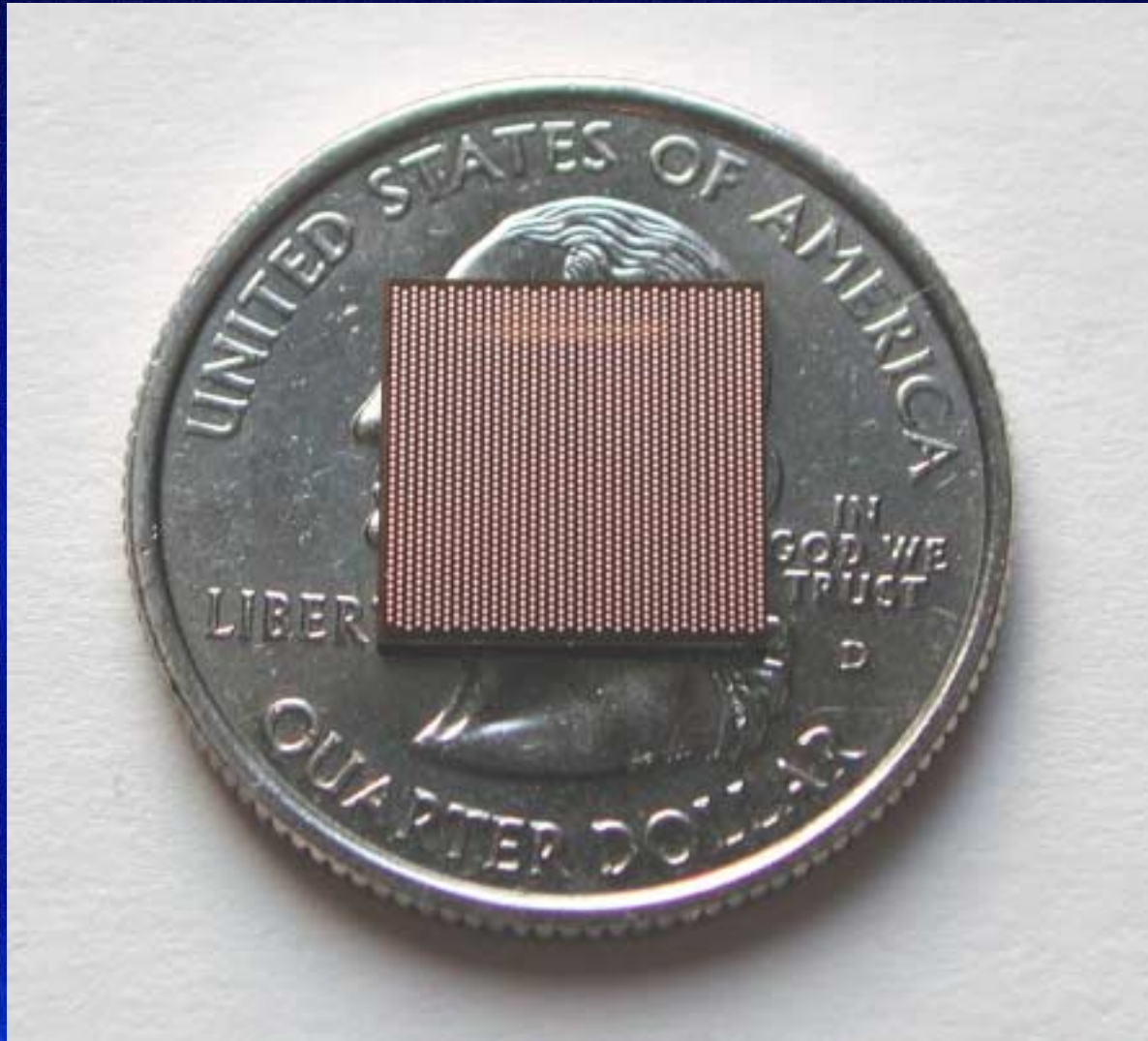
10.1 mm



10.8 mm

Perfect chips have been made with all 52 Mbits working

52 Mbit SRAM Chip



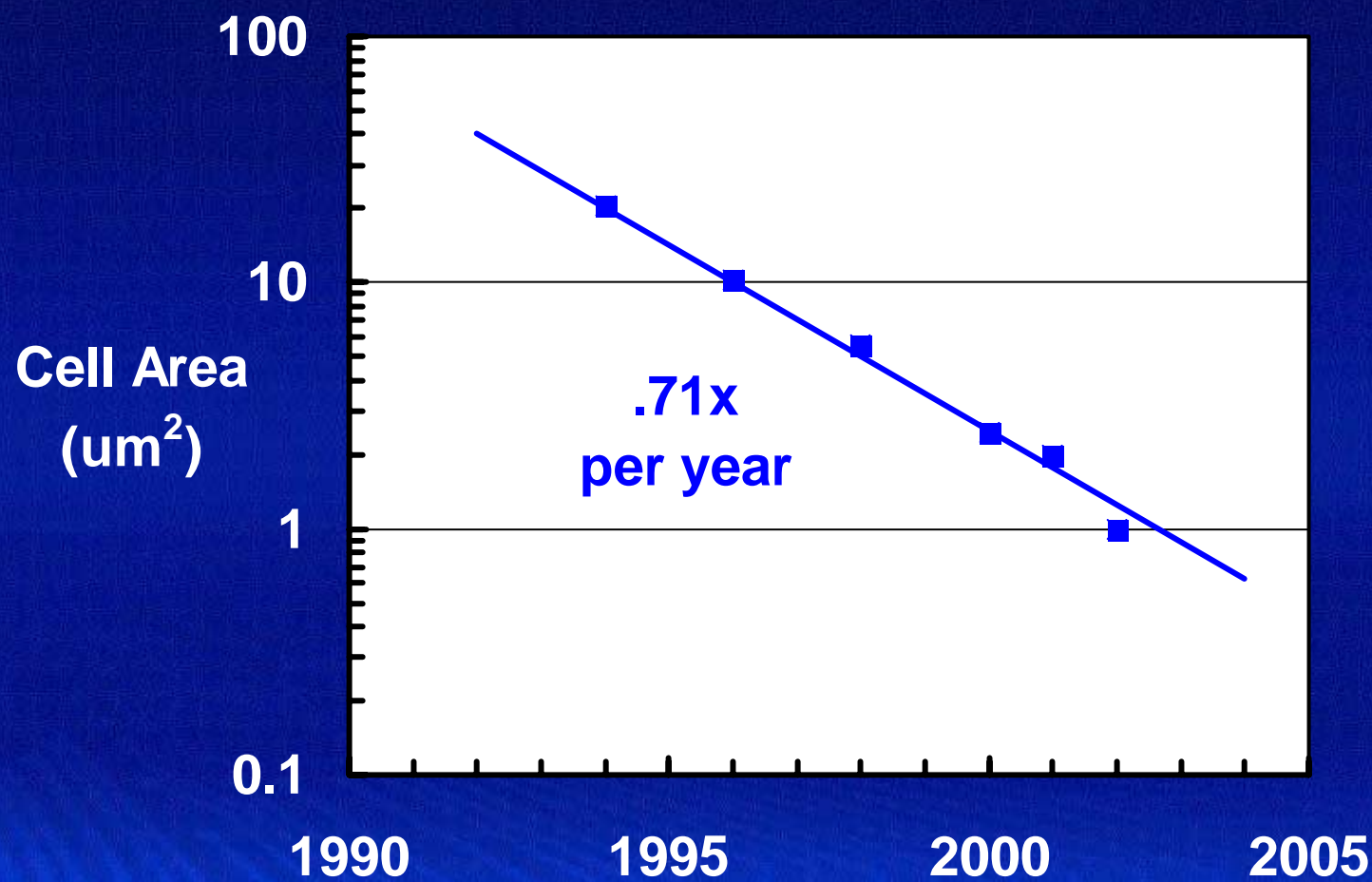
1 μm^2 SRAM Cell

- Smallest SRAM cell ever reported
- Packs six transistors in an area of 1 μm^2
- Small memory cell enables cost effective increase in microprocessor performance by adding more on-die cache memory



1 μm

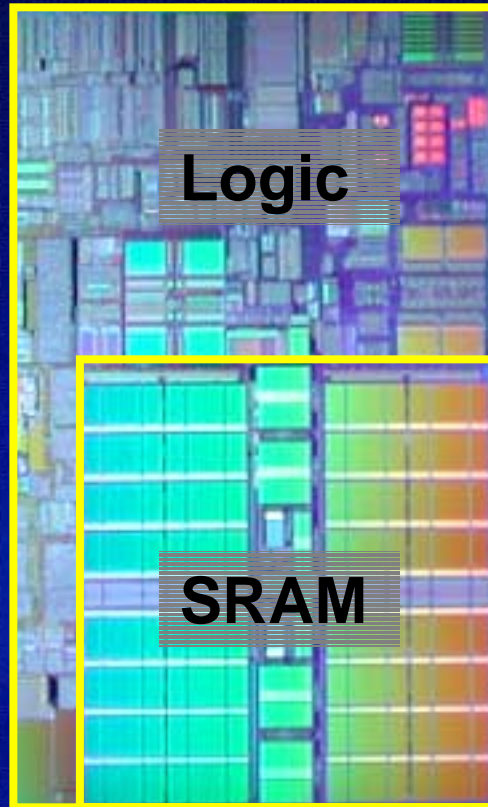
Intel SRAM Cell Size Decreasing Exponentially



Some Details

- This test chip was manufactured at Intel's 300 mm development fab, D1C, in Hillsboro, Oregon
- The process will be transferred to other 300 mm manufacturing fabs
- At 1 μm^2 , this SRAM cell is half the size of today's 0.13 μm generation SRAM cell
- Manufacturing makes use of next-generation 193 nm wavelength lithography equipment on critical layers
 - Non-critical layers will continue to use 248 nm lithography equipment

Same process for Logic and SRAM



0.13 μm
Pentium® III CPU
Example

- Modern microprocessors use the same transistors and interconnects for both logic and SRAM circuit blocks
- The process used to make 90 nm SRAM chips is the same process for 90 nm microprocessors

Summary

- Intel leads the industry in development of next-generation (90 nm) process technology
- Fully- functional SRAM chips with industry's smallest cell size (1 μm^2) and highest capacity (52 Mbit) have been produced
- The SRAM chip has 330 million transistors, showing that Intel is on track to deliver the 1 billion transistor microprocessor
- These SRAM chips demonstrate successful implementation of all 90 nm process features required for microprocessors, including fast transistors and 7 Cu interconnect layers

For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon